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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/908,941	07/20/2001	Masaki Hirase	010917	1043

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EXAMINER
KENNEDY, JENNIFER M

ART UNIT	PAPER NUMBER
2812	4

DATE MAILED: 06/13/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/908,941	Applicant(s) HIRASE ET AL.	
	Examiner Jennifer M. Kennedy	Art Unit 2812	

-- The MAILING DATE of this communication appears on th cov r sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) *1 and 2* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 July 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Claims 3-7 (3-8) in Paper No. 3 is acknowledged. The examiner notes that Claim 8 is also directed to a method of making a semiconductor device. Accordingly, Claim 8 will also be examined in this office action.

Drawings

Figure 1E should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims ~~1-4~~ 3-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Zhang et al. (U.S. Patent No. 6,303,458).

Zhang et al. discloses the method of making a semiconductor device comprising:

forming an element partitioning trench (42) and a mask aligning trench (40) in a semiconductor substrate (10);

depositing an insulation (40, 50) in the element partitioning trench and the mask aligning trench

applying a protective mask (60) on the insulation deposited in the element partitioning trench

etching the insulating deposited in the mask aligning trench to remove some of the insulation (see Figure 3B and column 4, lines 35-45); and

flattening an upper surface of the semiconductor substrate (see column 4, lines 55-60).

Zhang et al. also discloses the method of forming a coating (30) on the semiconductor substrate, wherein the coating has a pattern of openings corresponding to the element partitioning trench and the mask aligning trench and etching the semiconductor substrate using the coating as a mask to form the element partitioning trench and the mask aligning trench, wherein the insulation depositing step includes depositing the insulation without removing the coating (see column 3, line 65 through column 4, line 20).

Further, Zhang et al. also discloses wherein the semiconductor substrate is a substrate (10), the insulation is formed from oxide (40, 50), and the coating is formed from silicon nitride (30), the method further comprising the step of forming a oxide film (30) on the semiconductor substrate prior to the formation of the element partitioning trench and the mask aligning trench, wherein the coating is formed on the oxide film (see column 3, line 65 through column 4, line 4).

Claim Rejections - 35 USC § 103

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al. in view of Schoenfeld (U.S. Patent No. 6,127,245).

Zhang et al. does not teach the method of flattening is performed rotary grinding. Zhang et al. does teach the method of flattening by CMP. Schoenfeld discloses the method of utilizing a rotary grinder in CMP process. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a rotary grinding disc in order to create a uniform flat surface.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al. and Schoenfeld (U.S. Patent No. 6,127,245), in further view of Kuroi et al. (U.S. Patent No. 5,889,335).

Zhang et al. does not expressly disclose the method of forming the substrate of silicon, or the method of forming the insulation of silicon oxide, or the method of forming silicon oxide film on the semiconductor substrate prior to forming the silicon nitride layer coating.

Kuroi et al. discloses the method of utilizing silicon (1) as the substrate material, silicon oxide as the insulation material (2), and silicon oxide (3) as the pad oxide layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form these layers of these materials because they are preferred materials for their respective intended purposes.

Claim 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al. in view of Kuroi et al. (U.S. Patent No. 5,889,335).

Zhang et al. discloses the method of manufacturing a semiconductor device, comprising;

forming an oxide film (30) on an upper surface of a semiconductor substrate;

forming a silicon nitride film (30) on the oxide film;

partially removing the silicon nitride film and the oxide film;

forming an element partitioning trench and a mask aligning trench by etching the semiconductor substrate using a residue of the silicon nitride and silicon oxide films as a mask, wherein element partitioning trench and the mask aligning trench have substantially the same depths (see column 4, lines 4-26 and Figures1A, 1B);

simultaneously depositing a first layer of insulation and a second layer of insulation in the element partitioning trench and in the mask aligning trench, respectively (40, 50);

coating the first insulation with a protective mask (60);

etching the second insulation so that a step is formed between an upper surface the semiconductor substrate and an upper surface of the second insulation (see column 4, lines 45-55); and

removing the protective mask (see column 4, lines 55-60, and Figures 4A, 4B)

Zhang et al. further discloses the method wherein the first insulating and the second insulation are made of the same material (40, 50).

Zhang et al. does not expressly disclose the method of forming the insulation of silicon oxide, or the method of forming silicon oxide film on the semiconductor substrate prior to forming the silicon nitride layer coating.

Kuroi et al. discloses the method of utilizing silicon oxide as the insulation material (2) and silicon oxide (3) as the pad oxide layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form these layers of these materials because they are preferred materials for their respective intended purposes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (703) 308-6171. The examiner can normally be reached on Mon.-Fri. 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jmk
June 11, 2002

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800